Master's Thesis

Fast Startup and Low Power Crystal Oscillator for Internet-of-the-things Devices.

Yong-tae Shin

Department of Electrical Engineering

Graduate School of UNIST

2020

Fast Startup and Low Power Crystal Oscillator for Internet-of-the-things Devices.

Yong-tae Shin

Department of Electrical Engineering

Graduate School of UNIST

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

Fast Startup and Low Power Crystal Oscillator for Internet-of-the-things Devices.

A thesis/dissertation
submitted to the Graduate School of UNIST
in partial fulfillment of the
requirements for the degree of
Master of Science

Yong-tae Shin

Month/Day/Year of submission

Approved by

Advisor

Seong-Jin Kim

Fast Startup and Low Power Crystal Oscillator for Internet-of-the-things Devices.

Yong-tae Shin

This certifies that the thesis/dissertation of Yong-tae Shin

is approved.

12/03/2019

signature

Advisor: Seong-Jin Kim

signature

typed name: Jaehyouk Choi#1

signature

typed name: Kyu-ho Lee #2

Contents

Chapter 1.

Introduction

INTRODUCTION

IOT sensors in power hungry

In these days, IOT sensors are widely used. IOT sensors are small circuits are connected to internet, network systems.

For this reason, always on sensor's importance is also increases. Always sensors are same with their name, don't turn off and always turn on sensor. These sensors are widely used for sensing and turn on in-need sensors for example, conventional sensors. Most of a common example is Motion detection sensors this always sensor detect low frequency and low-resolution motion detection and turn on high resolution Cmos Image camera to get clean image.

These Always on sensors are extremely battery-limited due to this IOT sensors have minimal size and a large number of sensors hard to control their power 1 by 1.

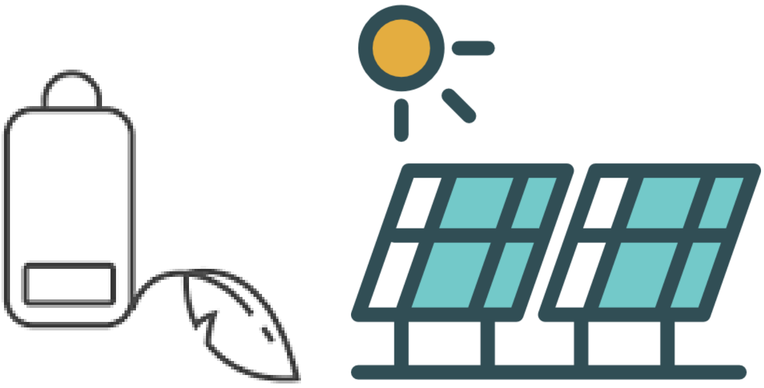

Fig1]Power sources in IOT sensors.

These power sources are limited in power consumption. Batteries are not replacement and energy harvesting has really little power making. For example, each generator generates 10mW/cm2 for solar power, 1200uw/cm2 for biofuel, 1000uw/cm2 for a thermoelectric generator. These are power generators for IOT sensors. [1]

Three-step method

Nowadays to decrease power consumption in IOT sensors, multi-mode operation is widely used.

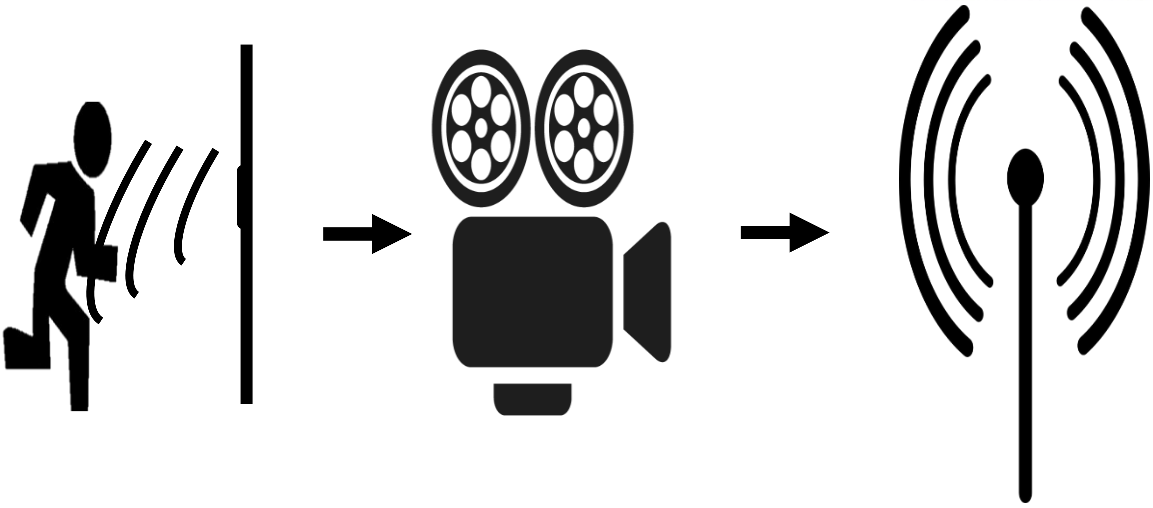

Fig2] Multi mode operation example

Moreover, to decrease power consumption, frequency scaling also widely used. In these conditions I suggest this three-step method.

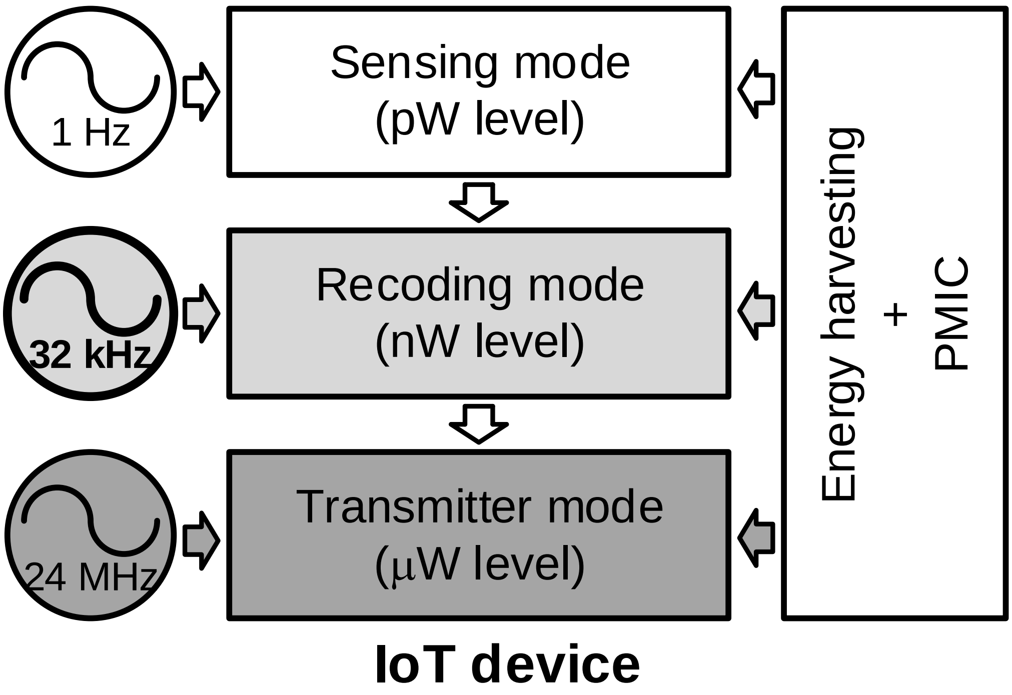

Fig3] Frequency scaling with the multi-mode operation example

In this system I focused to midrange frequency source. In recoding mode, a crystal oscillator is used for it. Because of the high accuracy and the low aging factor, I choose the pierce oscillator for this midrange oscillator. This circuit has Amp and crystal as resonator, some small noise is feedback to input and amplify to certain amplitude level. This circuit's power consumption is in 32.7khz frequency near 100nW. Many states of the arts show reduction method with this multi-step-scheme.[2][3][4]

Issues in Three-step

But In this proposed system, this power consumption is also can be problems. For this reason, turn off the clock for power saving. After then, turn on the clock when Sensing mode is on.

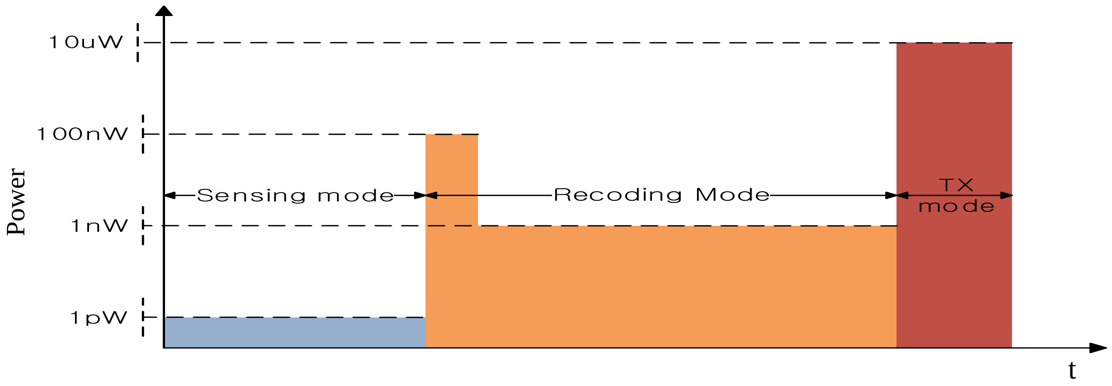

Fig4] Power budget in Crystal oscillator

But crystal oscillator has some problem to adjust this three-step method because of its slow start up. This circuit is black out when start up period. For this reason, this paper goal is Fasten startup

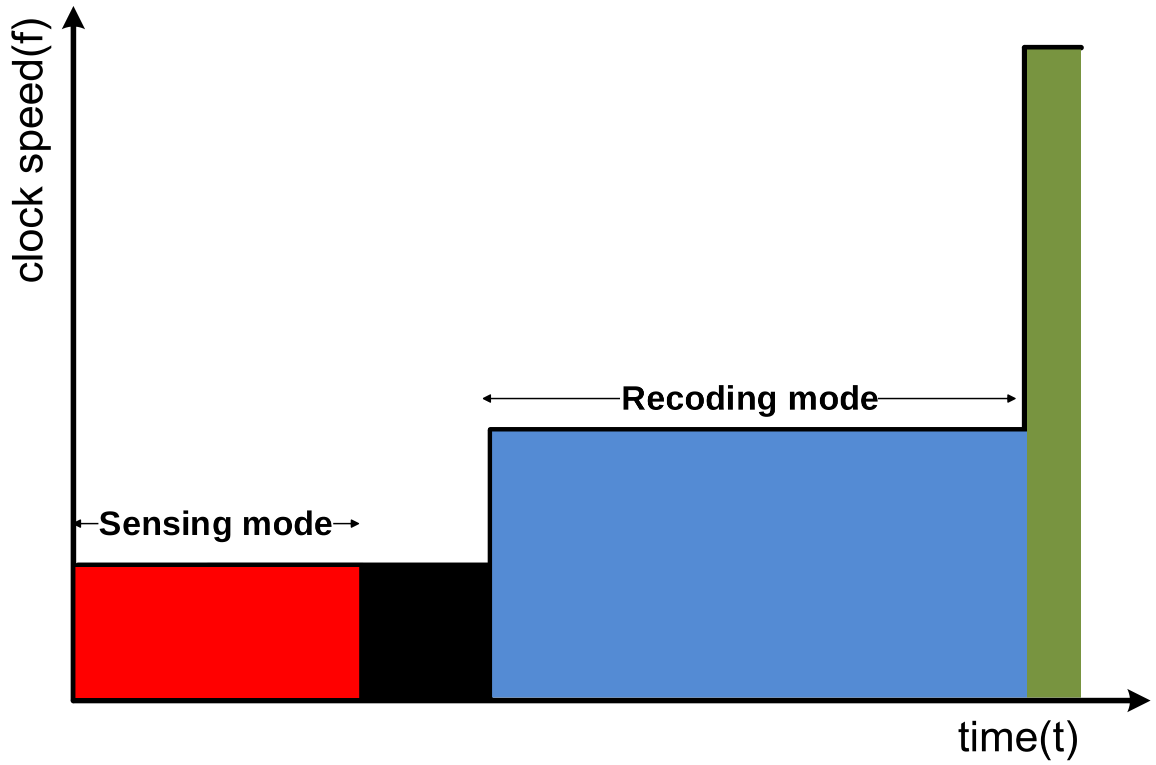

Fig5] Timetable of a proposed system

Chapter 2.

Theoretical & Mathematical Development

Oscillation Criteria

Oscillator is a circuit which are making frequency. Convert a DC signal to AC signal. This system is based on Barkuhausen criteria. Barkuhausen criteria include two conditions. 1.The gain is over 1 .And the phase difference is 360-degree. When these two conditions are meet, the signal is amplifying. This theorem lead to make positive feedback in the oscillator circuit. This is so called regenerative feedback. Most of circuits avoid this positive feedback, because of their stability. But an oscillator is using this positive feedback. In certain frequency, this positive feedback leads oscillation. These criteria are rewritten by these three blocks.

1.amplifier 2. feedback loop 3. Resonator

Oscillators are satisfying these conditions are really many. This are classified for some reasons. For example, using inverter delay for oscillator, ring oscillator, using RC delay for generate frequency, relaxation oscillator and use LC tank for resonator, LC oscillator.

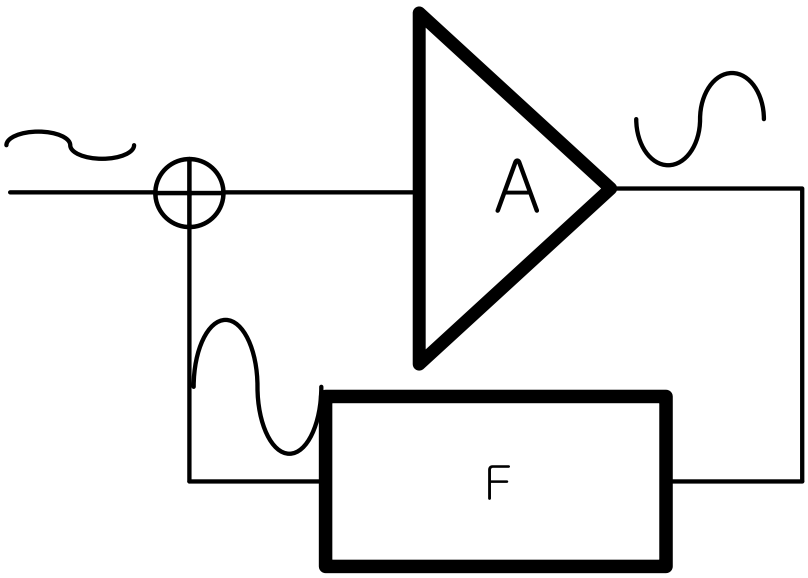

Fig6] Bakuhausen criteria

These criteria are rewritten in the equations in below.

$\mathrm{A_v} = \frac{Vout}{V_{in}}$ is open loop gain

Close loop gain is calculated by this way

$\mathrm{A_v}(V_{in} - FV_{out}) = V_{out}$

$\frac{V_{out}}{V_{in}} = G_v = \frac{A_v}{1+A_vF}$ When the feedback gain F has less than one(F<1). And it starts oscillation when AF>1. Which returns to unity (AF=1), once oscillations commence.

Oscillator classification-

I mentioned about classify by feedback loop. Another classification is output wave. One of it is sinusoidal oscillator and one of it is non-sinusoidal oscillator. In sinusoidal oscillator, LC RC quarts are included. Nonsinusoidal oscillators are composed with relaxation osc, Ring osc.

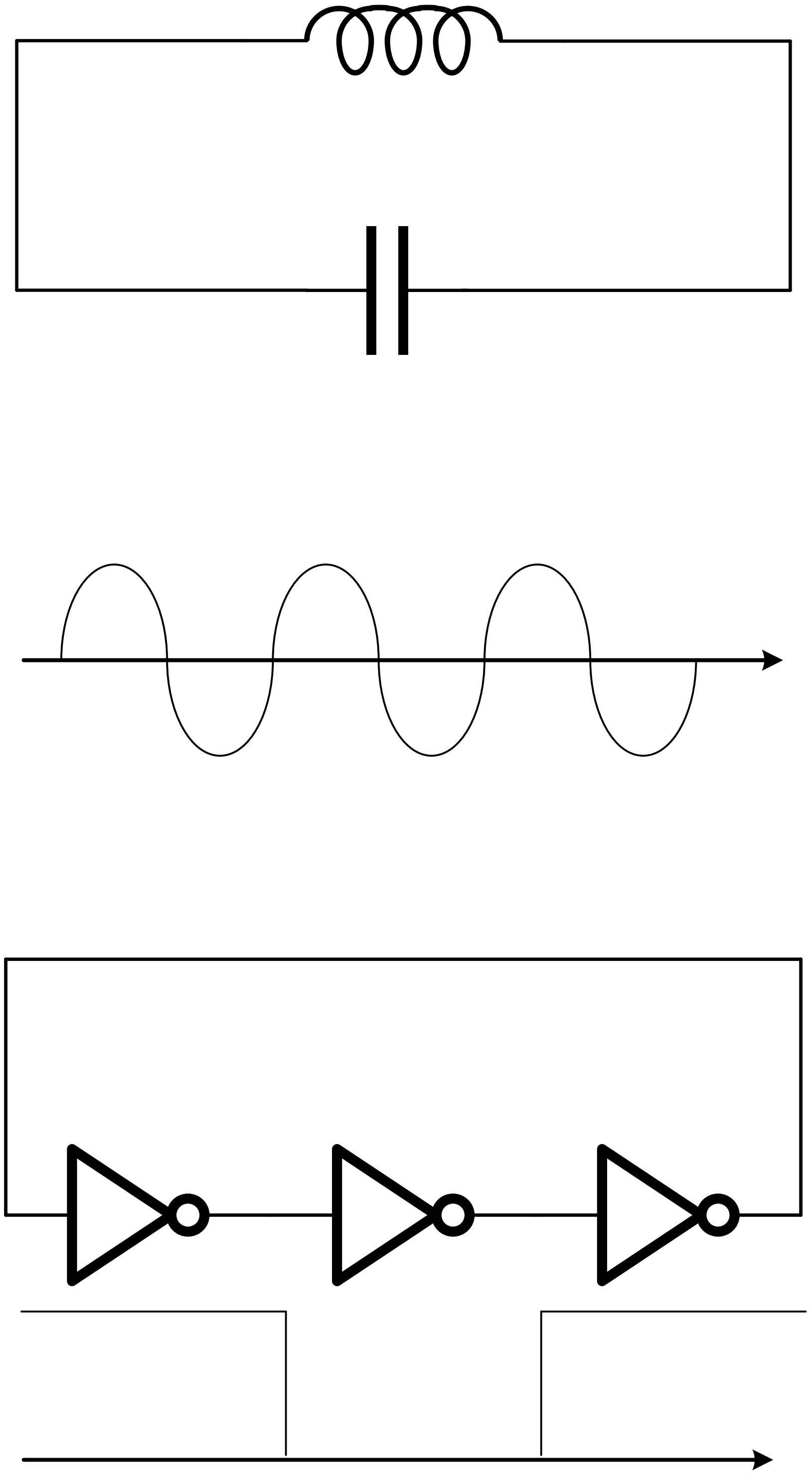

Fig7] Sinusoidal oscillator and Non-sinusoidal oscillator

Crystal Oscillator

Quartz are mechanically using piezo electric. Electric field and internal momentum difference make force, and this force are making frequency.

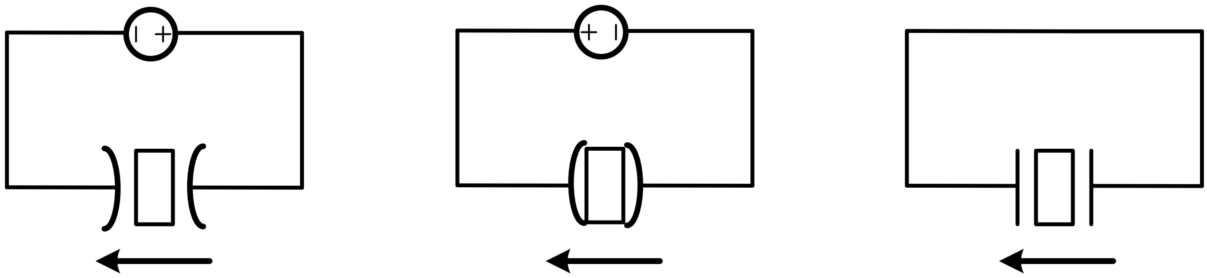

Fig8] Crystal in a Mechanical model

But we are used in circuit, this quartz mechanical properties are remodeled to circuits. Its modeling is similar to the LC circuit. We first show this LC oscillator.

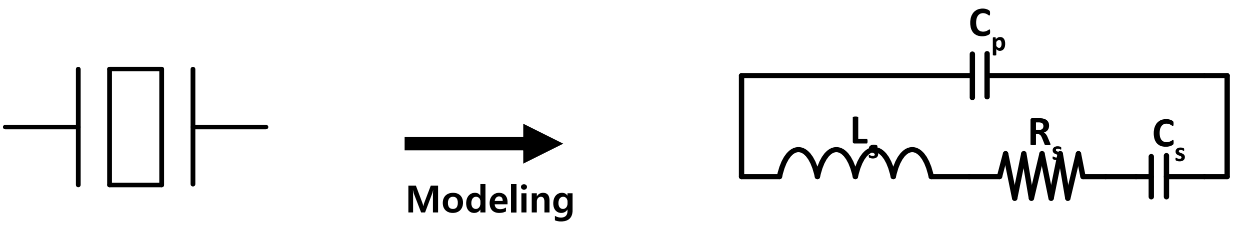

Fig9] Crystal in electrical model

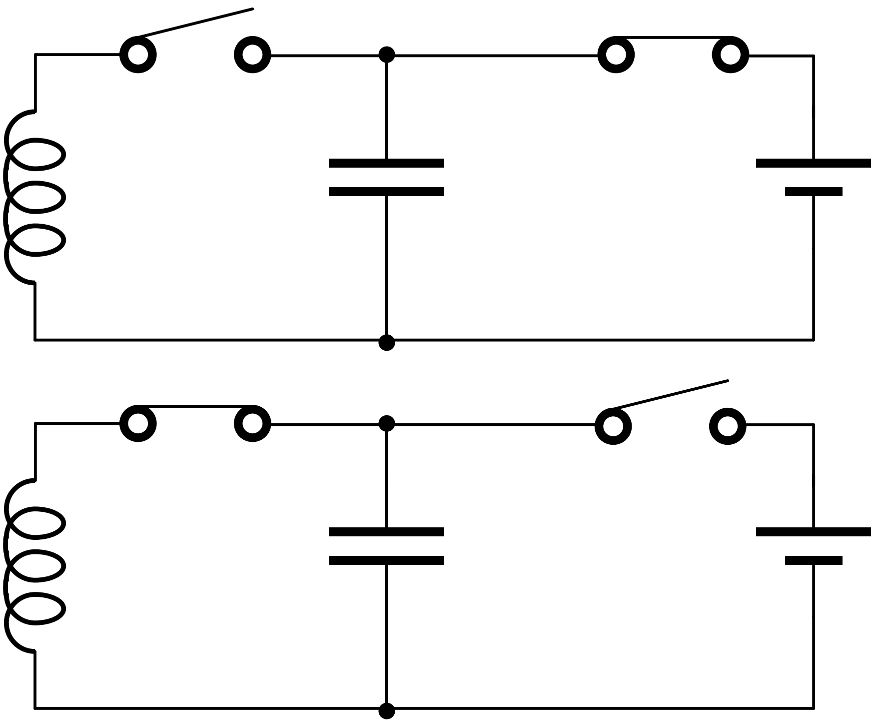

Fig10]LC oscillator schematic

At the first step, external battery charges a capacitor. The capacitor is full of charges. Then starts second steps, turn off to the voltage source and connect to the inductor. The capacitor is discharge and this current flow to an inductor. This current induces the magnetic field. At that time, this capacitor is totally discharged. This magnetic field generates current which can charge the capacitor. After this step, the capacitor has 180degrees difference in polarity when it has charged first. These sequential steps are repetitively occurring, sinewave is generated.

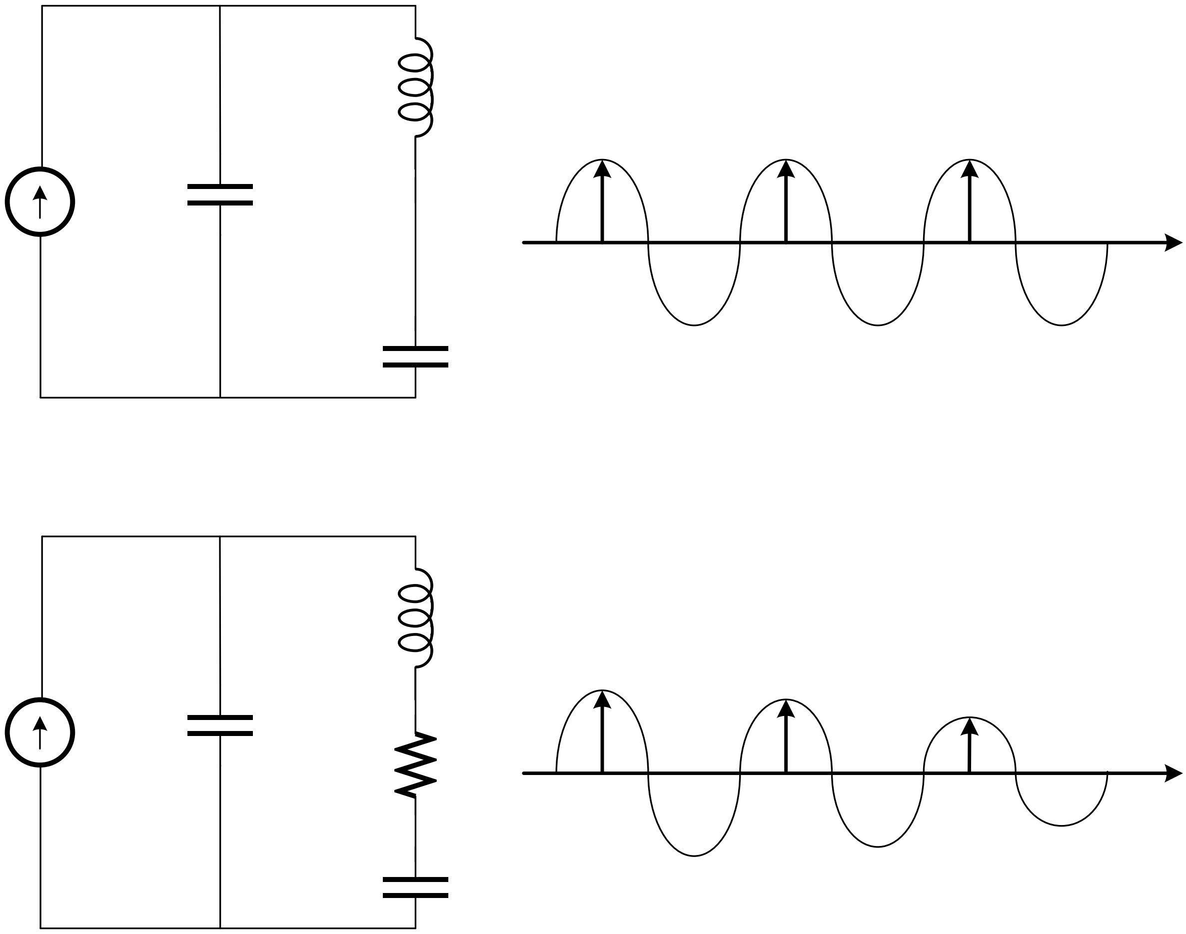

Fig11] RLC oscillator in ideal and lossy model

Negative Resistance

If this LC oscillator is ideal, oscillation is eternally work. But in actual effective series resistance has loss in thermal loss. This thing is called damping. Damping is as big as resistance. This resistance are needs to compensate with a negative value resistor. And this compensation resistance is called negative resistance.

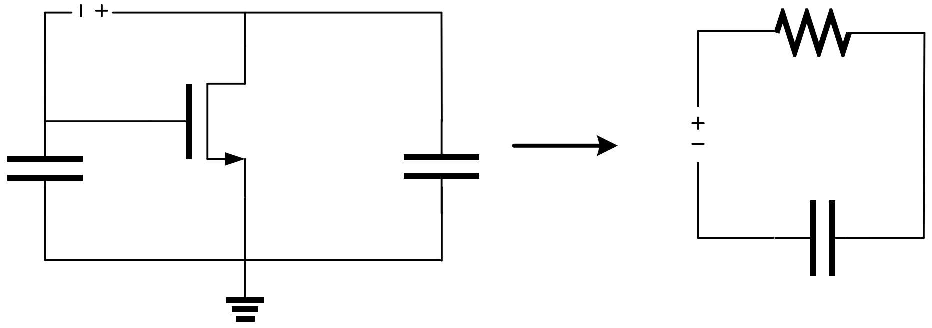

Fig12] Negative resistance modeling

Negative resistance is made by a capacitor connected to ground to output and ground to input. Input to output effective resistance is calculated like below.

$$\mathbf{V_{gs}} = -\frac{1}{C_1 w}\, \mathbf{I_x}$$

$$\mathbf{V_{ds}} = \frac{1}{C_2 w}\,(\mathbf{I_x} - \mathbf{g_m V_{gs}})$$

$$\mathbf{V_{ds}} - \mathbf{V_{gs}} = \mathbf{V_x}$$

$$\mathbf{R_N} \approx -\frac{g_m}{w_{osc}{}^2 (C_1 C_2)^2}$$

$$\mathbf{C}_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

This equation is shown to gm is bigger, Rn is bigger but in an actual crystal oscillator, it is wrong.

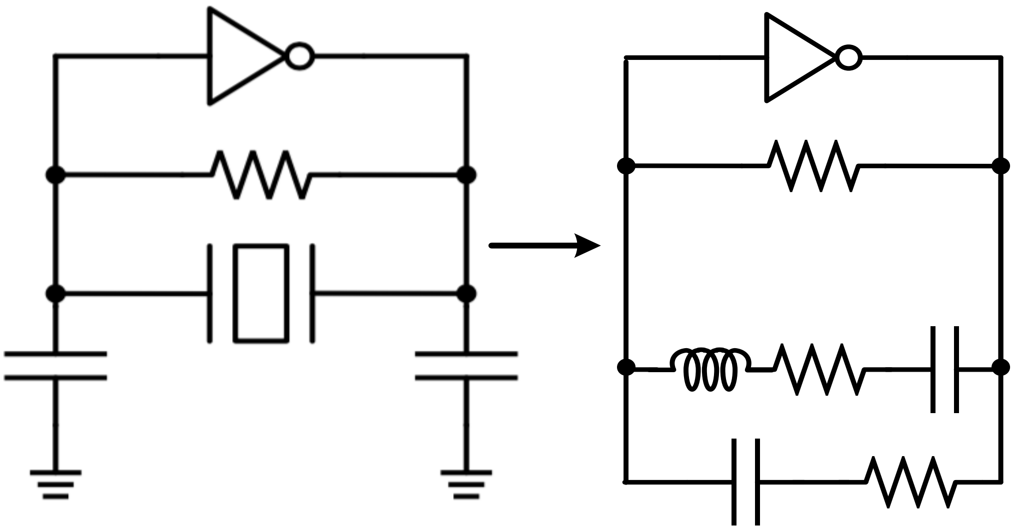

Fig12] Crystal oscillator modeling in negative resistance

Because of parallel capacitance, equation is changed. Gm optimal point is existing.

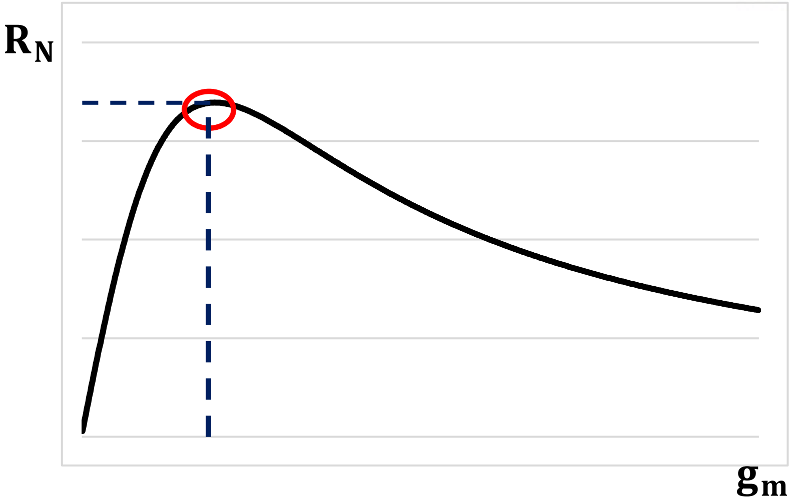

Fig13] Negative resistance in a crystal oscillator

Frequency of Oscillator

Now we see about Oscillation frequency in LC oscillator. This are setting where two impedances are same. This frequency is called resonance frequency.

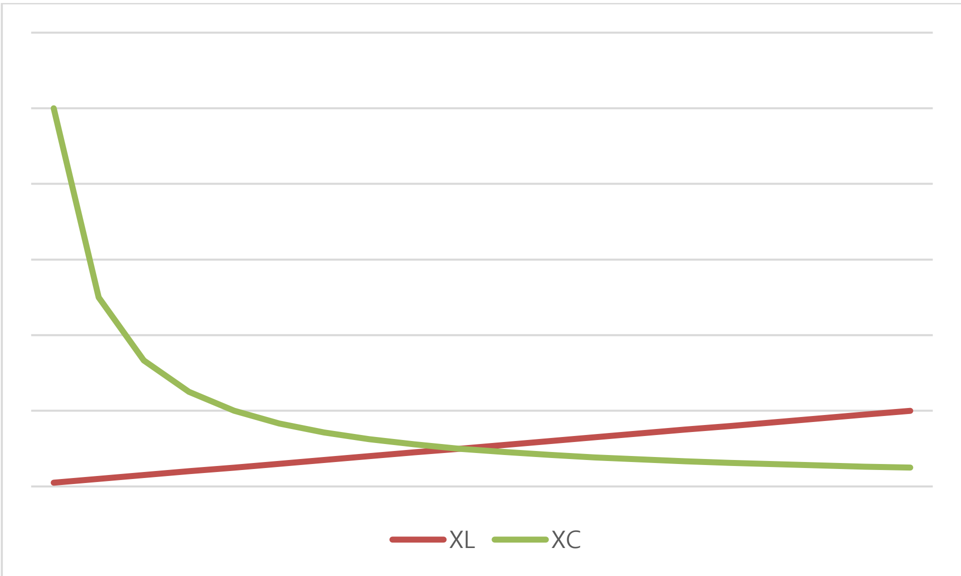

Fig14] Impedance vs Inductor and Capacitor

If the impedance of a capacitor are bigger than an inductor's. Circuit is capacitive. Otherwise circuit is inductive.

This frequency setting is a below equation.

$X_L = 2\pi f L$

$X_C = \frac{1}{2\pi f C}$

$f_0 = \frac{1}{2\pi (LC)^{\frac{1}{2}}}$

Chapter 3.

Fast startup Method

Fast startup

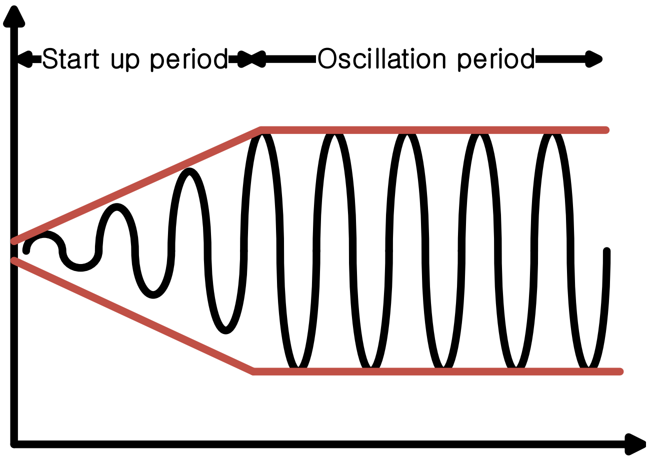

Fig15] Oscillation period

We see Oscillator modeling above. We can know feedback gain is stronger, an initial signal is higher, Startup period is shortened. Now we know we have two plans for fasten startup

1. increase the initial signal
2. increase the amplifier gain

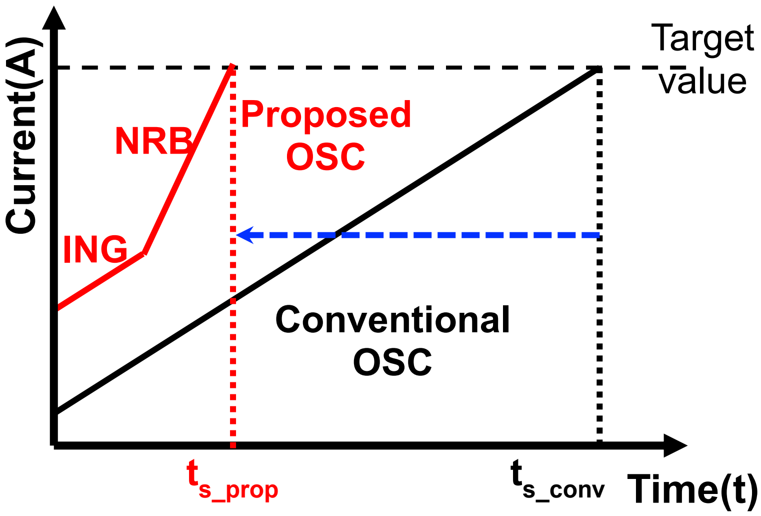

Fig16] Fasten startup time with two methods are adjusted.

ING

Increase initial value, we select which oscillator is better. I choose Three-types of oscillators which are in next.

These oscillators are Voltage mode ROSC, current mod ROSC and quadrature ROSC. These oscillators' information is in the below table.

	Frequency range (Hz)	**Vdd range**	**Area (mm^2)**	**Power consumption**	**Startup time**
Voltage-mode ROSC	1k~10M	0.5~2(V)	0.01~0.1	0.05~50(uW)	10us~100us
Current-mode ROSC	100~100M	0.35~2(V)	0.03~0.1	0.01~1(uW)	Instantly
Quadrature ROSC	10M~10G	1~6(V)	~ 0.03	uW~mW	1us~1ms

Table1] ING comparison

This circuit is required fast startup, low power consumption, 32.7khz signal. For these requirements, we select current mode ROSC.

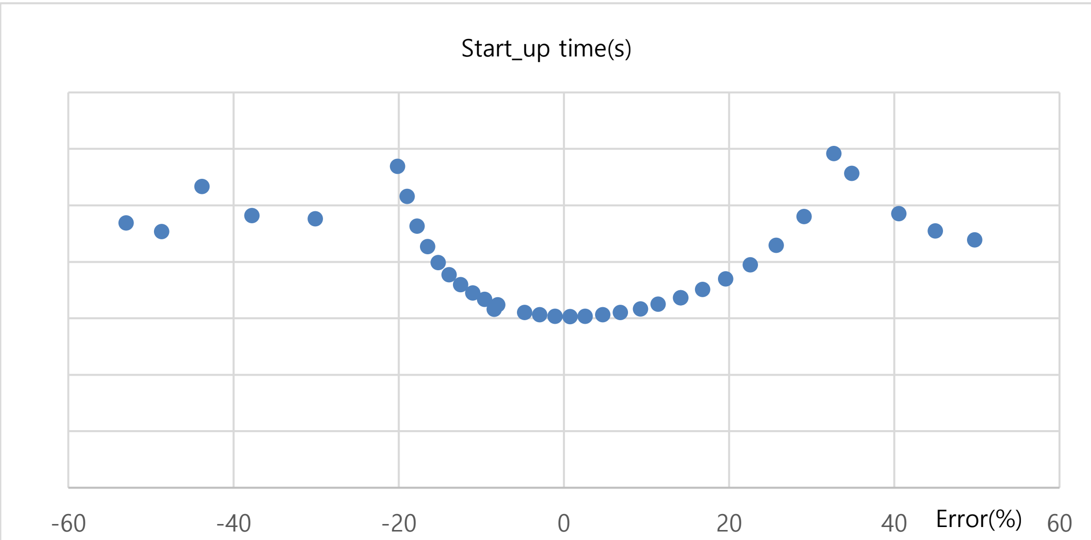

Fig 18] Injection frequency error vs start up time graph

Injection signal which has frequency error within 10%, is effective for startup shortened.

NRB and duty cycling

Another method is Increase gain. In fig 13. optimal gain point is existing. Match circuit gain to optimal point.

These methods are also increase power consumption. To decrease power consumption use duty cycling.

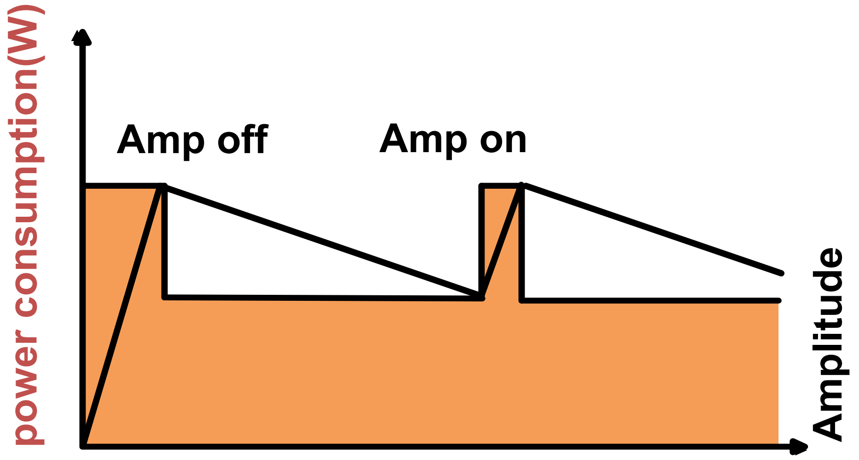

Fig 19]duty cycling for power saving

Chapter 4.

Proposed Design

Overall schematic

In need of fast start-up and low power consumption, I make this layout for the proposed circuit. Looking at the expression startup time equation in next, to reduce startup we need increasing Imint, initial current, wXo, Crystal Frequency, and Rn , Negative Resistance and Decreasing of Rm, Motional resistance of Crystal and Q, a Quality factor of Crystal.

$$\mathrm{T_{start}} = \frac{2Q}{W_{XO}} * \frac{1}{\frac{R_n}{R_m} - 1}\left[\log\frac{I_{M,ss}}{I_{M,int}}\right]$$

due to frequency of the Crystal Wxo are determined by target frequency, can not change it. And decreasing Quality fac0tor Q also decrease Frequency accuracy. Rm motional resistance of crystal is material specification. It is hard to change. Because of these reasons, to Decrease startup time I choose the method to change Rn and Im, int. In this way I suggest the scheme shown on Fig19. with three circuits. (fig2) First, Initial Noise Generator (ING) which increases the initial signal level. Second, Negative Resistance Booster (NRB) for increase speed of amplifying. Third, to reduce power consumption use Auto Reference Power Gating (ARPG)

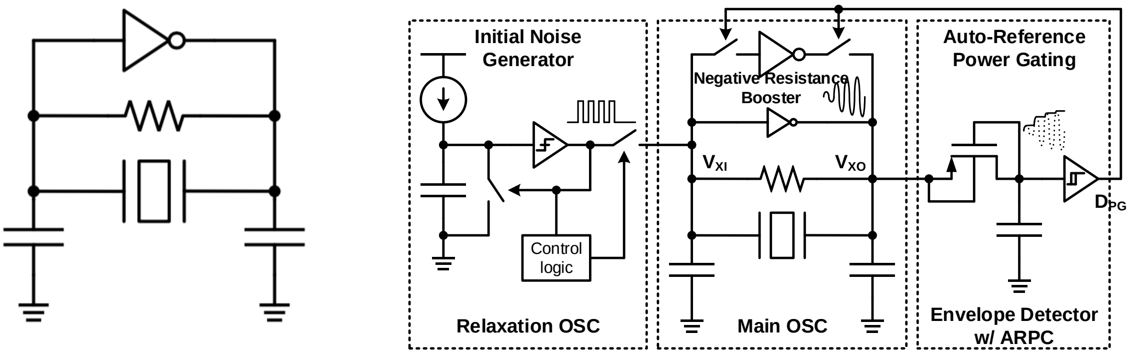

Fig19] Proposed design

ING

Due to a high Q factor of crystal, very narrow band frequency signals are only accepted, and other frequencies are rejected. We use crystal which has tens of thousands Q factor. So, it only accepts very specify frequency. For Adding initial noise level, that noise frequency must meet in that band. In this way we use several schemes for inject specify frequency are proposed. It is in fig3. At first to compensate PVT variation, I use 2T transistor reference PTAT voltage. In this way I can make linearly dependent in temperature variance in very low supply (0.5V in this circuit).

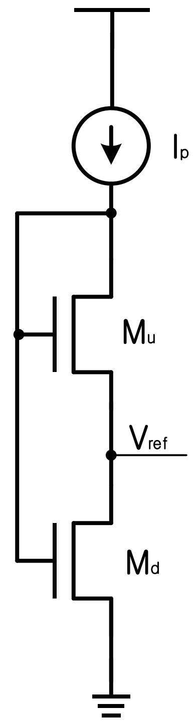

Fig20]PTAT voltage generator

$I_{sub} = \mu_0 C_{ox} \frac{W}{L} (m-1) V_T^2 \exp\left(\frac{V_{gs}-V_{th}}{\eta V_T}\right)(1-\exp\left(\frac{-V_{ds}}{V_T}\right))$

Assume $\frac{-V_{ds}}{V_T} \cong 0$ when $V_{ds} > 60mV$

$V_{ref} = V_{gs,M_d} - V_{gs,M_u} = \eta V_T ln(K_{M_u}/K_{M_d})$

K=ratio of W/L

[5]

This PTAT Voltage reference is compared with integrated Cinb. Current are flow into Cinb which are made by Resistor Rinb with CTAT coefficient. This current is PTAT coefficient. Sufficient charge is integrated in Cinb, than Voltage of Cinb are higher than PTAT reference. Compare MOSFET source are connected to Cinb. Gate-source voltage are decreases and mosfet are in cut-off region. Then output node goes to vdd. This result feedback to Cinb, Cinb resets to ground. And theses cycle makes frequency. In equation V/I=Ct, I and V both have CTAT coefficient their voltage variance are attenuation. Furthermore, to compensate rest of temperature variation, I sweep frequency by make Cinb 2bit CDAC. With control logic. And I choose duty 50%. Because it has highest amplitude in central frequency.

$retancgular\ wave\ function(duty(D)) = \Sigma \frac{2A}{n\pi} \sin(dn\pi)$

This Noise injector can't make duty 50% signal because a long time to integration and this signal is reach to certain level, it goes down instantly with reset-switch ON. For this reason, I add D-Flipflop to make 50% duty signals. And this add-on makes frequency halve. The Noise-Injector target frequency was twice of crystal frequency. This ROSC has additional power consumption. But this ROSC running time is under 100us. It is smaller than 0.01% of total start up-time (1.26s).This ROSC's power consumption portion is a negligible. After making 4 pulses, control logic turns on power gating this ROSC. In this way I can prevent useless power consumption.

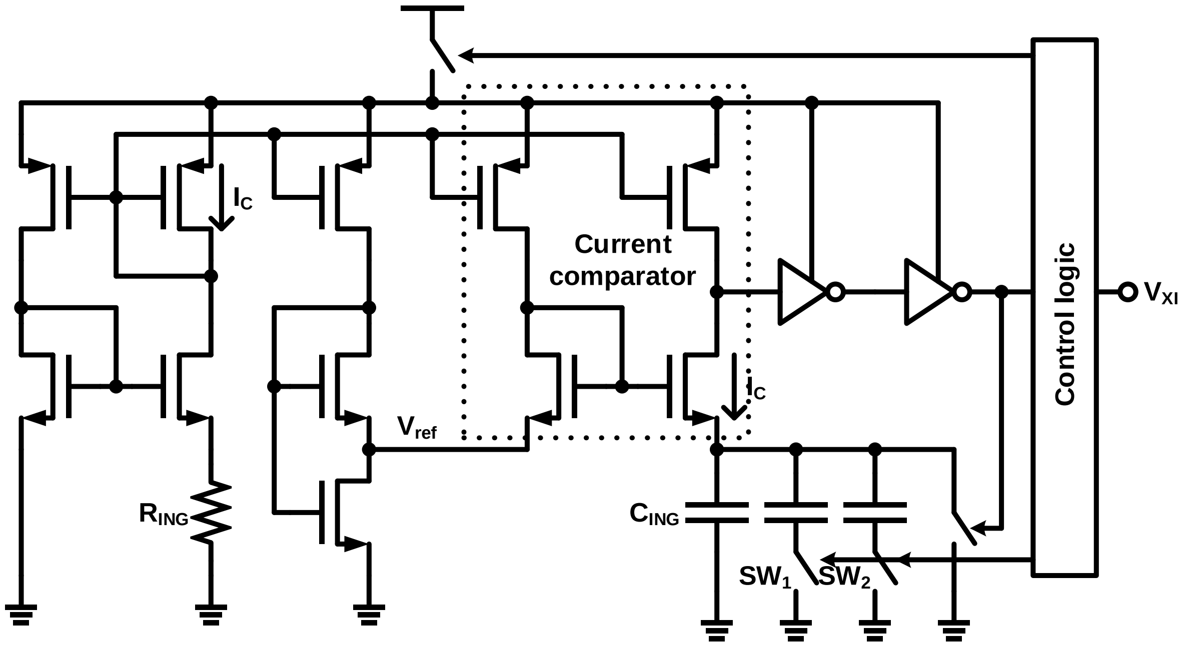

Fig21]ING schematic

NRB+ARPG

From startup time equation Negative Resistance also has highly relation with start-up. For this reason, Increase Negative resistance are also important for reducing startup time. Negative Resistance are shown in the next equation.

$\mathrm{R_N} = -\frac{gm}{C_L C_L}$,

[6]

We can see in this equation, transconductance(gm) and load capacitor (C_L) are highly influence to negative resistance ($\mathrm{R_N}$). But load capacitors are also related with Pulling Factor As we can see in equation in below, Q Factor is decreases. And adjust capacitor DAC for startup time and free running time cannot be useful due to large size load capacitor up to ~tens pF is needed.

$Pulling\ Factor = \frac{C_m}{C_p + 2C_L}$

[7]

In these reasons, only remain methods are increases gm. But increased gm induced power consumption increasing. To compensate this power consumption increases, turn on an additional circuit only while startup and other times turn off power consumption. I suggest schematic in figure 4. Use two inverters which has different size in parallel. In a start_up period, turn on both of these inverters turn on for achieve high transconductance. Higher transconductance lead to faster start_up. When start_up is over. Inverter output swing is high enough, envelope detector which connect to output node can tracking output. This envelope detector voltage is reach to certain level, which is Auto Reference power gating circuit's toggle point, turn off additional inverter. Thanks to this operation, I can reduce power consumption after startup is over. This operation also affects to ARPG. Decreases Pmos size to decrease trip point of IT. This operation is designed for reducing input level sensitivity can help near certain level, Prevent On-off switches work too often switch which can consume in very high frequency. This ARPG has a larger pmos/nmos size ratio than NRB's and main inverter's. For this reason, this toggle point is higher than inverter's operation voltage.

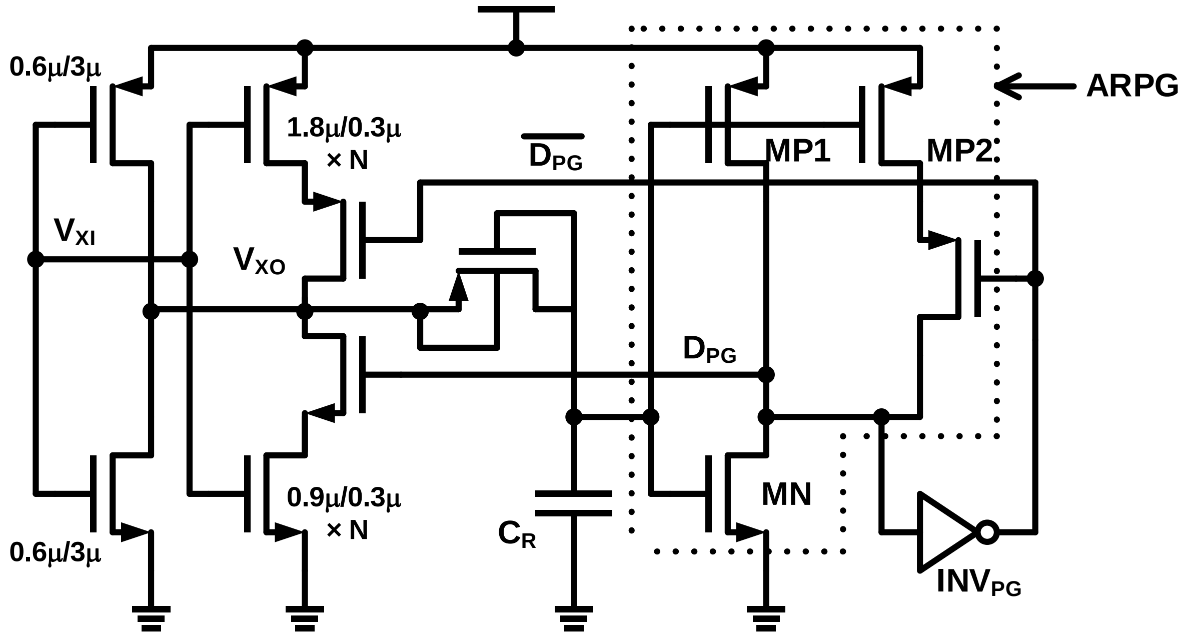

Fig22] NRB+ARPG schematic

Chapter 5.

Measurement Result

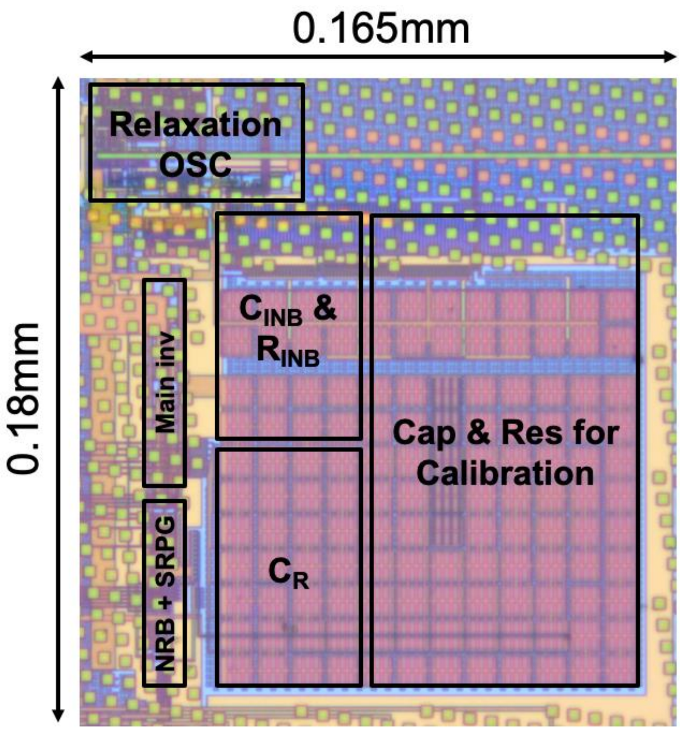

Fig23] Die photo

This proposed Xo with APRG was fabricated using 130nm CMOS process. Fig23 shows a die photo and its size is 0.165*0.18mm including capacitor and resistor for calibration.

These experiments are normally experienced in 0.5V supply and main size 0.6u/3.0u without any significant value are mentioned.

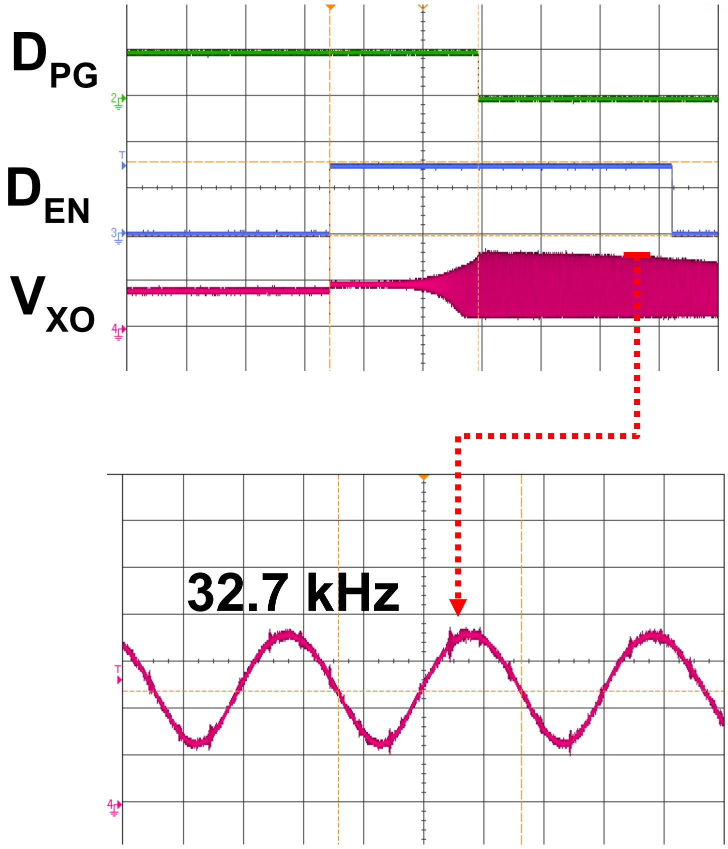

Fig24] Overall operation of crystal oscillator

Fig24 shows operation of this circuit. Enable signals (Den) set high when the startup starts. Oscillator output voltage (Vxo) swing levels are increases. Vxo reaches certain level, ARPG output signal so called power gating (Dpg) goes to low NRB terminated. This period, main invertor only turn on and oscillator output swing decaying start. Fig 24 also shows output frequency is 32.768khz, target frequency.

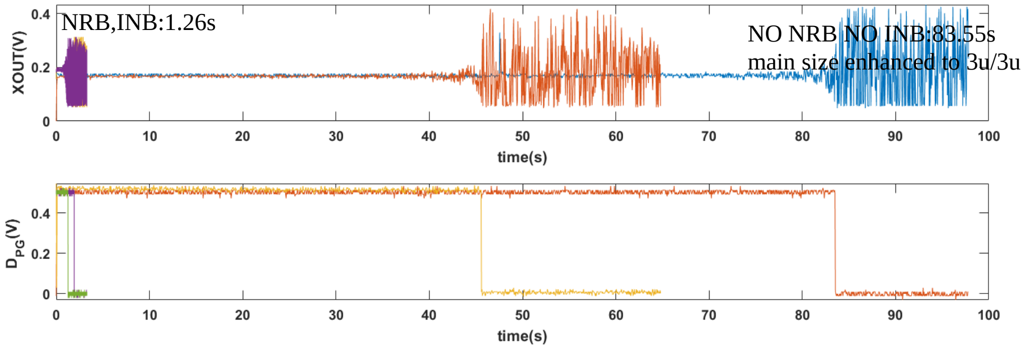

Fig25]startup time for various method approach

Fig25 shows startup times in different conditions. The blue graph shows enhanced the main inverter's size to 3u/3u without NRB. Without initial noise injection startup time is 83.55s. The orange graph shows enhanced main inverter with ING, without NRB startup decreases to 45.6s. With Noise injection only, startup time reduced to 35%. The purple line shows reduced the main inverter size to 0.6u/3u and use the NRB method. Without ING time decreases to 1.92s. Increasing gm method can reduce startup time 97.8%. The orange line is reduced the main inverter size to 0.6u/3u and using both method ING and NRB. Startup time reduced to 1.26s. It is 98.5% decreases compare with use nothing of this startup method.

Size of NRB uses as unit value which has 0.6u/0.3u W/L ratio, can control with an external calibration signal at most N=16. NRB size is counter proportional to the startup time. Fig. 26 and Fig. 27 shows startup time are proportional to the duty cycle. Because of a large power consumption period is shortened.

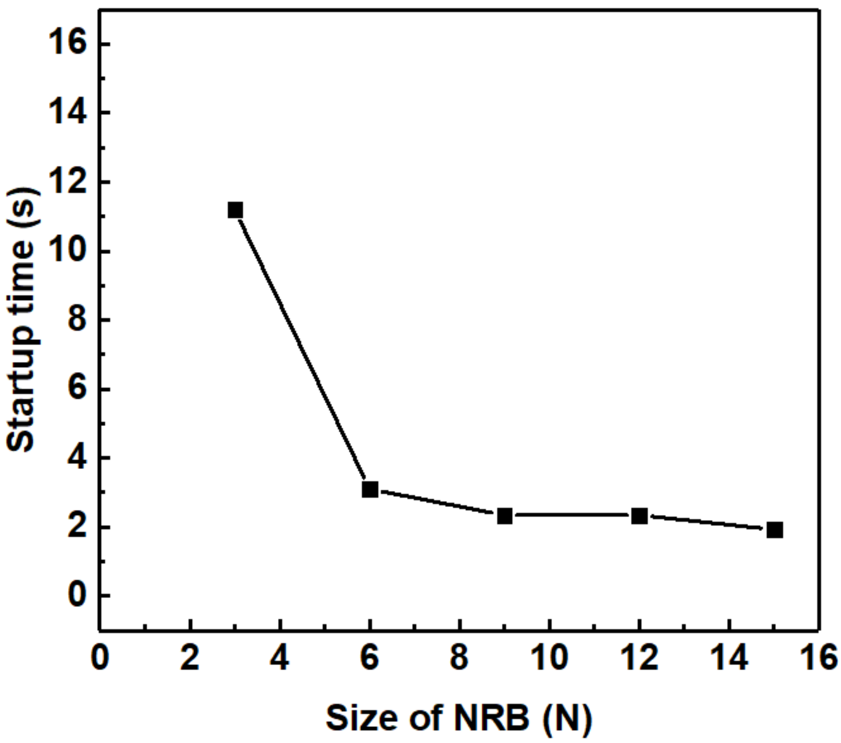

fig 26] Startup time vs Size of NRB

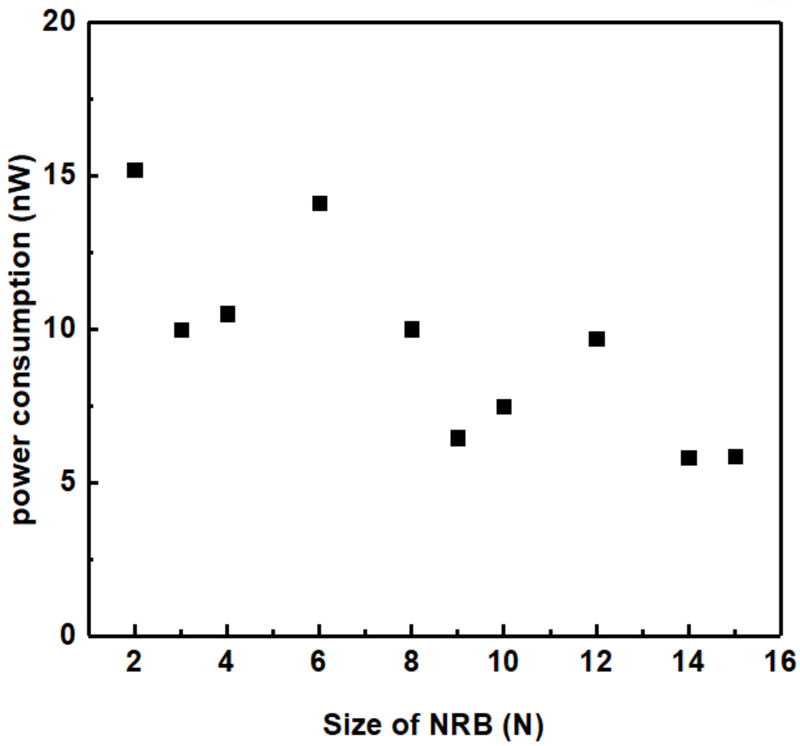

fig27] Power consumption vs size of NRB

Size of Main inverter has W/L ratio 0.2u/3u as unit value, can control an external calibration signal at most size =16. As the main size increase decaying speed is slow down, duty cycle is decreases as decaying speed decreases. Especially over N=4, in 0.5V supply. Power consumption decreases as duty cycle decreases. In fig 29 and fig 30.

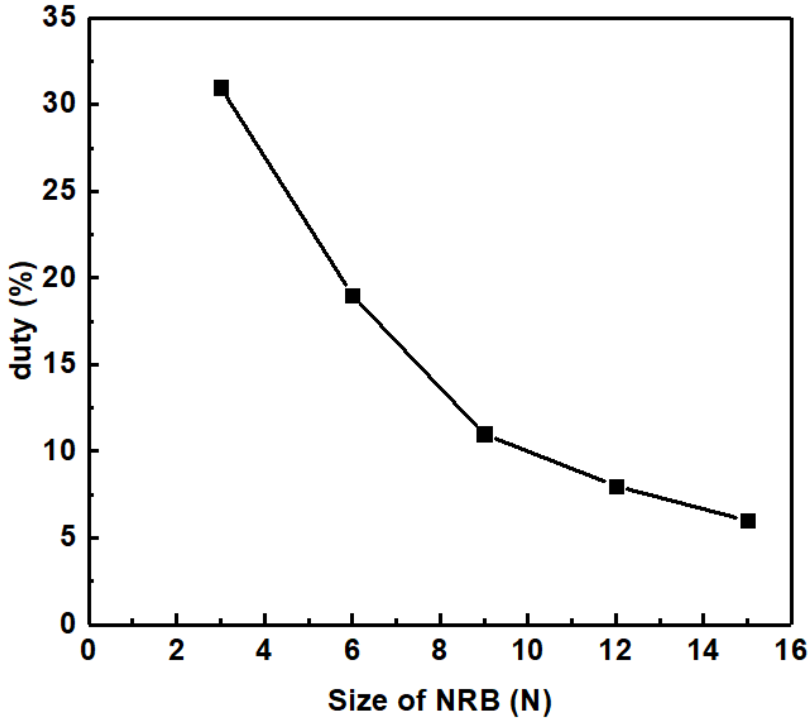

fig28] Duty cycle vs size of NRB

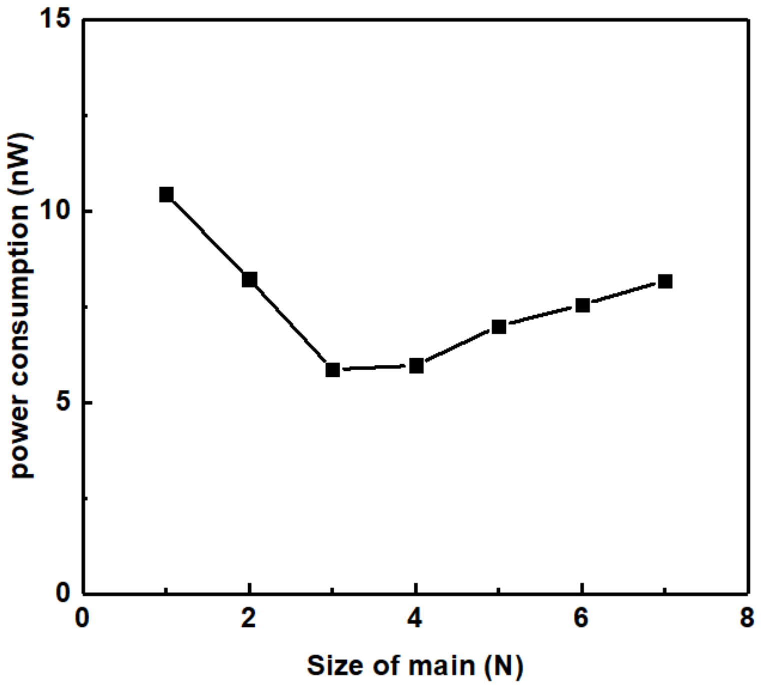

fig29] Power consumption vs size of main inverter

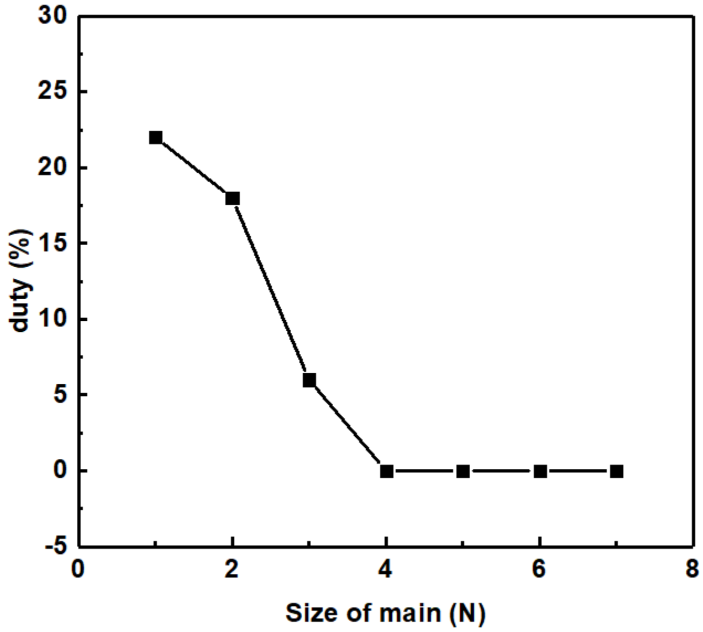

Fig30] Duty vs size of main

Fig 31 shows how to work Auto Reference Power Gating and Duty Cycling. Due to a difference of Pmos / Nmos Size in Comparator and NRB inverter, switching level is automatically controlled. This voltage graph shows voltage level is difference as on voltage and off voltage.

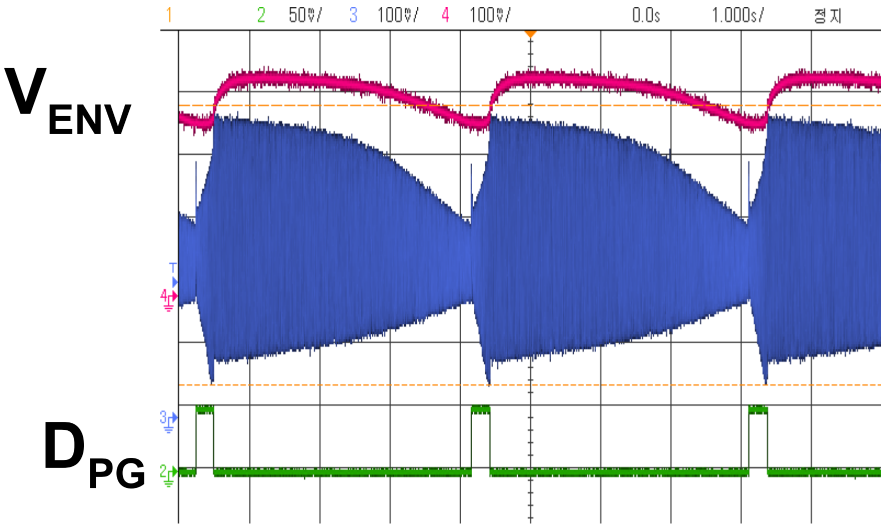

Fig31] Duty cycling and auto reference setting

In fig 32, Compare with 2 cases, the one is oscillator starts in natural, main size N=7 which are stats without NRB and ING. Second is main size N=3 and use duty cycling ING and NRB. This graph shows 0.45 V to 0.6V and power consumption is decreases as 33%

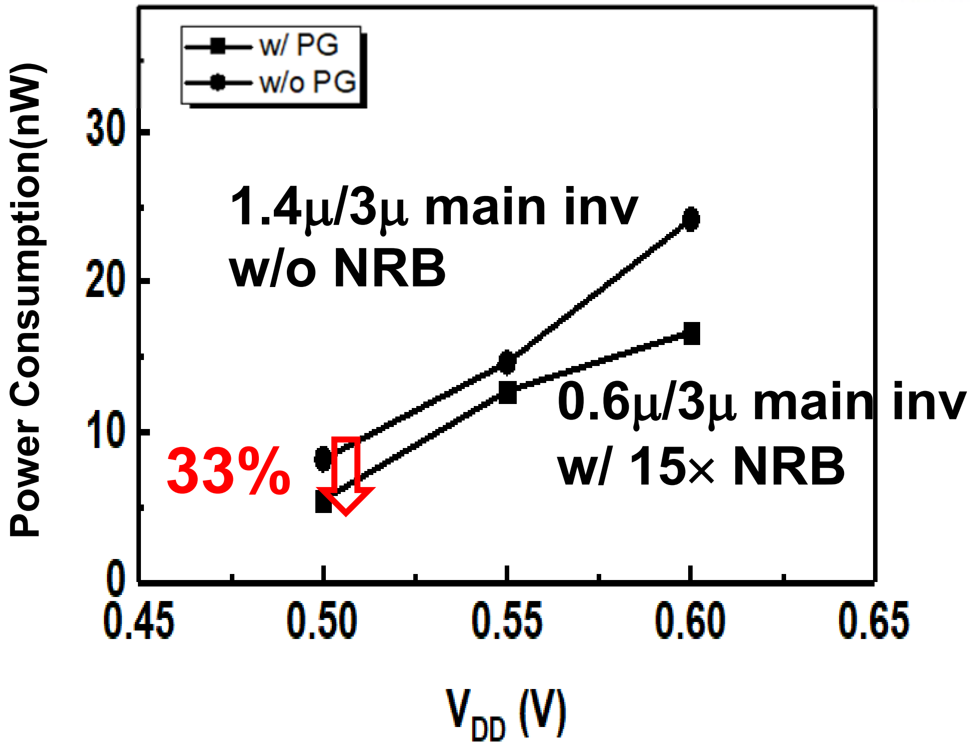

Fig32] Power consumption vs duty cycling

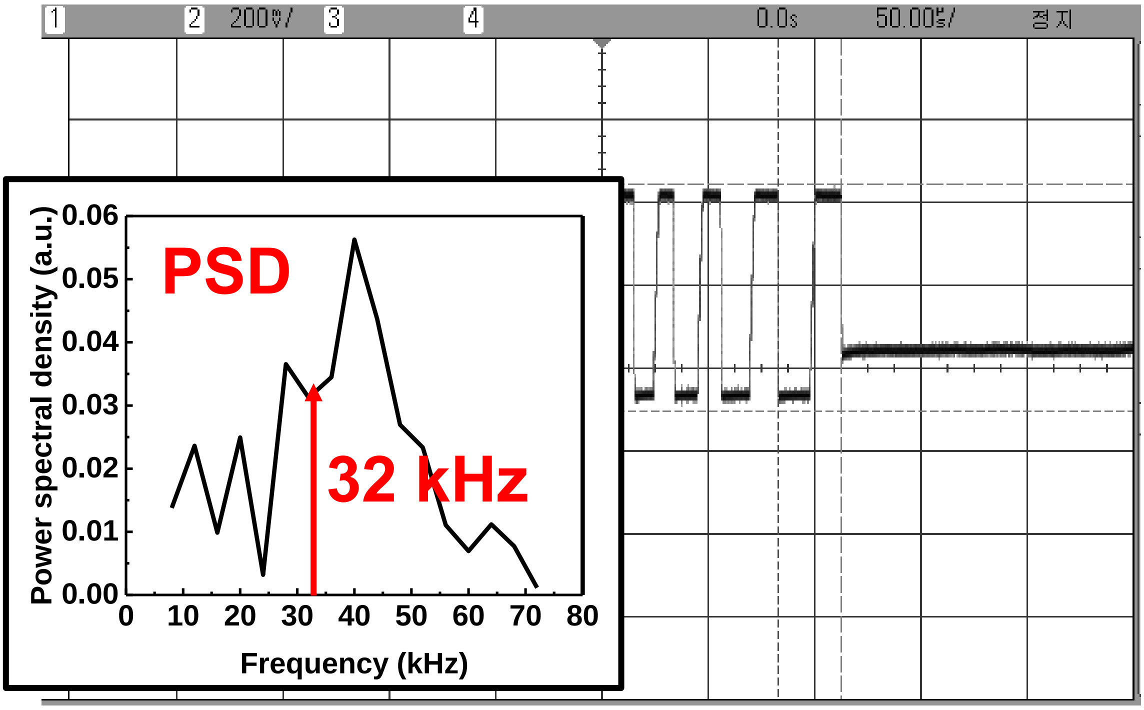

Fig 33] ING frequency chirping and PSD analysis

Fig 33 shows 4 pulse injection of ING. Each frequency is 33.7k/37.7k/45.9k/54.3kHz pulses. This injection signals are analysis in Furrier transform. PSD are in 32.7khz are enough.

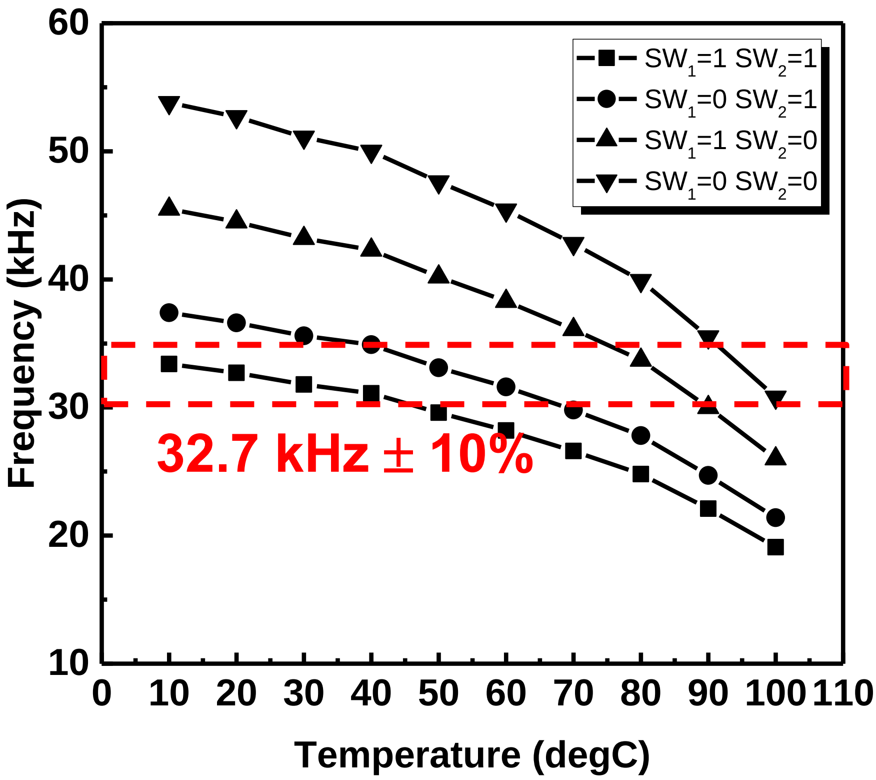

Fig34] ING frequency vs temperature

Fig34 is temperature variation of ING. Thus, temperature variation is occurred in CTAT variance. But with chirping injection signals. One of the injection frequencies has +- 10% error, comparing with target frequency, we can know it is enough for injection

	JSSC2016[4]	ISSCC2012[8]	ISSCC2014 [3]	This work
Technology	0.13 μm	28 nm	0.18 μm	0.13 μm
Operating frequency	32 kHz	32 kHz	32 kHz	32 kHz
Area (mm^2)	0.0625	0.03	0.3	0.03
V_{DD} (V)	0.3–0.9	0.15–0.5	0.92–1.8	0.5–0.7
Power consumption (nW)	1.5 @ 0.3 V	1.89 @ 0.15 V	5.58	5.85 @ 0.5 V
Startup time (s)	31 @ 0.3 V	N/A	N/A	1.26 @ 0.5 V

Table2] Comparison table

Comparing with previous works, it has a same power consumption with previous works and has 30times faster start up time.

Chapter 6.

Summary& Further work

Todays, many IOT devices are used in our life. But this IOT devices are suffered from battery issues. To reduce power consumption in IOT devices, many of us use multi-step-method and frequency sailing. I propose the circuit which has short startup and low power consumption clocks. I use two proposed methods called ING and NRB, these two methods induced start-up time shorter as 98.5%. But this result is start-up time >1sec.This time is also two much for devices. Startup-time need further decrease. Additionally, changing load capacitor to decrease Q factor can be shortened startup time 10X faster.

References

Ref1) Sally Safwat , " MISIMO: A Multi-Input Single-Inductor Multi-Output Energy Harvester Employing Event-Driven MPPT Control to Achieve 89% Peak Efficiency and a 60,000x Dynamic Range in 28nm FDSOI",ISSCC2018

Ref2) Keng-Jan Hsiao MediaTek, Hsinchu, Taiwan ,"A 1.89nW0.15V Self-Charged XO for Real-Time" ,ISSCC2014

Ref3) Dongmin Yoon, Dennis Sylvester, David Blaauw, University of Michigan, Ann Arbor, ," A 5.58nW 32.768kHz DLL-Assisted XO for Real-Time Clocks in Wireless Sensing Applications", MIISSCC2012

Ref4) Aatmesh Shrivastava, Divya Akella Kamakshi, and Benton H. Calhoun, "A 1.5 nW, 32.768 kHz XTAL Oscillator Operational From a 0.3 V Supply", JSSC2016

Ref5) Ken Ueno ,"CMOS Voltage Reference Based on the Threshold Voltage of a MOSFET" ,Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials

Ref6) E. A. Vittoz, M. G. R. Degrauwe, and S. Bitz ,"High-Performance Crystal Oscillator Circuits: Theory and Application", JSSC, Vol. 23, No. 3, June 1988

Ref7) Ming Ding, Yao-Hong Liu, Yan Zhang, Chuang Lu, Peng Zhang, Benjamin Busze, Christian Bachmann, Kathleen Philips, "A 95µW 24MHz digitally controlled crystal oscillator for IoT applications with 36nJ start-up energy and >13× start-up time reduction using a fully-autonomous dynamically-adjusted load",ISSCC2017

Ref8) K.-J. Hsiao, "A 1.89nW/0.15V self-charged XO for real-time clock generation",*IEEE ISSCC,* 2014,